(54)【発明の名称】　画像信号処理装置

【特許請求の範囲】

【請求項1】原画像における各画素の再配分画像信号レベルを記憶する再配分用記憶手段の所定位置におけるM個の画像信号レベルの和Smと一画素前に処理したときに発生した配分誤差enを求め、画像信号の最大値Cを（nレベル-1）で除算したレベルに設定した所定の画像信号レベルCnの配分数Nと残差Aを求め、前記所定の画像信号レベルCnを1/2に除算した半値画像信号レベルCn/2と前記残差Aとを比較し、前記残差Aが前記半値画像信号レベルCn/2と等しいか又は大きいとき、前記配分数Nに1を加えた新たな補正配分数N+1と、また前記残差Aが前記半値画像信号レベルCn/2より小さいとき、そのまま前記配分数Nと決定する配分値演算手段と、原画像における各画素の画像信号レベルを記憶する順位付用記憶手段の前記所定位置と対応した画素の一部に近傍補正

量Ebを加えたM個の画素の画像信号レベルの値により画素順位を決定する順位決定手段と、前記画素順位により前記配分数N（又はN+1）と前記M個の画素数との関係がN（又はN+1）＜Mのとき、前記所定の画像信号レベルCnと0を割り当て、前記配分数N（又はN+1）と前記M個の画素数との関係がN（又はN+1）＝Mのとき、前記所定の画像信号レベルCnを割り当て更に、前記配分数N（又はN+1）と前記M個の画素数との関係がN（又はN+1）＞Mのとき、すでに前記画素順位に従って配分した前記所定の画像信号レベルCnにN（又はN+1）個の画像信号レベルCnを再び前記画素順位に従って加算して決定した結果を、前記再配分用記憶手段の所定位置のM個の画素に割り当てて多値化画像信号レベルとする再配分手段と、順位付補正量Ecを記憶する補正量記憶手段の前記所定位置と対応する画素の近傍の順位

付補正量Ec'から前記近傍補正量Ebを演算し前記順位決定手段に与え、さらに前記順位付補正量Ecと前記順位付用記憶手段の画素の一部の画像信号レベルと前記多値化画像信号レベルとから新たな順位付補正量Ecを演算する順位付補正手段と、前記配分値演算手段により求めた総和Sと前記配分分数N（又はN＋1）と残差Aとから配分誤差enを演算し、前記配分値演算手段に与える配分誤差演算手段とを具備した画像信号処理装置。

【請求項2】順位付補正手段は近傍の順位付補正量Ecの平均値Ecaを求め、係数$1/2^L$（ただし、Lは正の整数）を乗算して、近傍補正量Ebを演算し前記順位決定手段に与えることを特徴とする請求項1記載の画像信号処理装置。

【請求項3】順位付補正手段は近傍の順位付補正量Ecの平均値Ecaを求め、係数$1-1/2^m$（ただし、mは正の整数）を乗算して、順位付用記憶手段の画素の一部の画像信号レベルを加算しさらに多値化画像信号レベルを減算して、新たな順位付補正量Ecを求めることを特徴とする請求項1記載の画像信号処理装置。

【発明の詳細な説明】

産業上の利用分野

本発明は階調画像を数レベル程度の記録系で多値再生する機能を備えた画像信号処理装置に関するものである。

従来の技術

近年、日常業務におけるOAやファクシミリの発展と伴に、従来の文字や線画に代表される白／黒2値の画像のほかに階調画像のより忠実な再現の要望が強まっている。特に、数階調程度のプリンタに対する擬似中間調再現の要望がされている。

従来よく知られている方法に多値組織ディザ法がある（小野他、多値ディザ法による中間調信号表示、テレビジョン学会全国大会、1978年）。

第4図（a）は、0、1/2、1が記録できる3値化の組織ディザ法の例である。同図において401は入力信号の端子、402は後述する比較器の出力端子、403は入力信号の端子401から入力される画像信号と後述する閾値マトリックス404の閾値信号とを比較して出力する比較器、404は比較器403に閾値信号を与える閾値マトリックス405はタイミング信号入力端子である。同図（b）は3値化の4x4閾値マトリックスの構成を示す。

動作原理は、一画素を2分割して1/2以下の濃度は0か1/2で、1/2以上の濃度は1で記録する。従って0～1/2の間に分布する閾値マトリックスAijと1/2～1の間に分布する閾値マトリックスBijを用意し、注目画素の濃度Iijを比較することにより記録レベルPijが定まる。即ち、

$Iij<Aij$ ⇨ $Pij=0$

$Aij\leq Iij\leq Bij$ ⇨ $Pij=1/2$

$Bij<Iij$ ⇨ $Pij=1$

と表すことができる。

一般に、記録できるレベル数Lはマトリックスサイズを

nxn、多値化のレベル数をmとすると、$L＝（m-1）\times n^2＋1$で表される。4×4の3値化の場合は$L＝（3-1）\times 4^2＋1＝33$レベル表すことができる。同サイズのマトリックスで4値は49、5値は65、6値は67レベルを表すことができる。さらにマトリックスサイズを8×8とすると、4値では193レベルを表現できる。

発明が解決しようとする課題

さて、上記多値組織ディザ法は小さなマトリックスサイズでも1画素を複数に分解することによって多くの階調レベル数を表現できるが、更に高階調性を得ようとするとマトリックスサイズを大きくする必要がある。高分解能を得るためにはマトリックスサイズを小さくしなければならないという矛盾があるため階調特性と高分解能特性の両立に限界があり問題であった。

本発明は、上記課題を解消し、数階調程度の濃度を表現できる記録、表示系に対して多値化画像信号を出力し高品位に再生できる画像処理信号処理装置を提供するものでる。

課題を解決するための手段

本発明は、

（1）原画像における各画素の再配分画像信号レベルを記憶する再配分用記憶手段の所定位置におけるM個の画像信号レベルの和Smと一画素前に処理したときに発生した配分誤差enを求め、画像信号の最大値Cを（nレベル-1）で除算したレベルに設定した所定の画像信号レベルCnの配分数Nと残差Aを求め、前記所定の画像信号レベルCnを1/2に除算した半値画像信号レベルCn/2と前記残差Aとを比較し、前記残差Aが前記半値画像信号レベルCn/2と等しいか又は大きいとき、前記配分数Nに1を加えた新たな補正配分数N＋1と、また前記残差Aが前記半値画像信号レベルCn/2より小さいとき、そのまま前記配分数Nと決定する配分値演算手段と、

（2）原画像における各画素の画像信号レベルを記憶する順位付け用記憶手段の前記所定位置と対応した画素の一部に近傍補正量Ebを加えたM個の画素の画像信号レベルの値により画素順位を決定する順位決定手段と、

（3）前記画素順位により前記配分分数N（又はN＋1）と前記M個の画素数との関係がN（又はN＋1）＜Mのとき、前記所定の画像信号レベルCnと0を割り当て、前記配分数N（又はN＋1）と前記M個の画素数との関係がN（又はN＋1）＝Mのとき、前記所定の画像信号レベルCnを割り当て、更に、前記配分数N（又はN＋1）と前記M個の画素数との関係がN（又はN＋1）＞Mのとき、すでに前記画素順位に従って配分した前記所定の画像信号レベルCnにN（又はN＋1）個の画像信号レベルCnを再び前記画素順位に従って加算して決定した結果を、前記再配分用記憶手段の所定位置のM個の画素に割り当てて多値化画像信号レベルとする再配分手段と、

（4）順位付補正量Ecを記憶する補正量記憶手段の前記所定位置と対応する画素の近傍の順位付補正量Ecから前

記近傍補正量Ebを演算し前記順位決定手段に与え、さらに前記順位付補正量Ecと前記順位付用記憶手段の画素の一部の画像信号レベルと前記多値化画像信号レベルとから新たな順位付補正量Ecを演算する順位付補正手段と、（5）前記配分値演算手段により求めた総和Sと前記配分数と残差Aとから配分誤差e_nを演算し、前記配分値演算手段に与える配分値演算手段とを具備した画像信号処理装置とを設けたものである。

作用

本発明は上記手段により、原画像の濃度レベルに応じて再生画像の数階調濃度レベルの黒画素密度を決定すると共に原画像の濃度レベル変化に応じて再生画像の黒濃度レベルの画素配置を決定し、数階調程度を表現できる記録、表示系に対して、滑らかで高品位な擬似中間調画像再現をするものである。

実施例

第1図は本発明の一実施例における画像信号処理装置のブロック図を示すものである。本実施例では前記発明の構成（1）、（2）、（3）におけるM個を4個とし、構成（5）における近傍の順位付補正量Ecは4個とする説明にしている。説明の都合上、各画素には次のような記号を付与している。

構成（1）、（3）の4個の画素はR_{00}、R_{01}、R_{10}、R_{11}とし

構成（2）の4個の画素はO_{00}、O_{01}、O_{10}、O_{11}とし

構成（5）の近傍の順位付補正量Ecの記憶位置はEc_1、Ec_2、Ec_3、Ec_4とし、新たな順位付補正量Ecの記憶位置はEc_5とする。各画素の画像空間上の対応位置はR_{00}とO_{00}とEc_5が同じ位置に対応する。

前記各記号グループを走査窓と定義し、R_{00}、R_{01}、R_{10}、R_{11}を走査窓Wrとして、O_{00}、O_{01}、O_{10}、O_{11}を走査窓W_0とし、Ec_1、Ec_2、Ec_3、Ec_4、Ec_5を走査窓Weとする。第1図において各走査窓はそれぞれの対応する記憶手段上を原画像の主走査とともに右方向へ移動していくものとする。

第1図において、1は原画像を走査し画像信号レベルを出力する原画像走査手段、2は原画像走査手段1の出力信号である原画像の画像信号レベルと後述する再配分手段の出力信号である再配分用画像信号レベルとを入力として記憶し、走査窓Wrの4個の画素R_{00}、R_{01}、R_{10}、R_{11}の画像信号レベルを出力とする再配分用記憶手段、3は再配分用記憶手段2の出力信号である走査窓Wrの4個の画素R_{00}、R_{01}、R_{10}、R_{11}の画像信号レベルと後述する配分誤差演算手段10の出力信号である配分誤差e_nを入力して、加算した和Sを求め、画像信号の最大値Cをn値−1で除算した画像信号レベルCnの配分数Nと残差Aを求め、画像信号レベルCnを1/2に除算した半値画像信号レベルCn/2と残差Aとを比較し、残差Aが半値画像信号レベルと等しいか又は大きいとき、配分数Nに1を加えた新たな補正配分数N＋1を、又残差Aが半値画像信号レ

ベルより小さいとき、そのまま配分数Nを出力する配分値演算手段、4は走査手段1の出力信号である原画像の画像信号レベルを入力として記憶し走査窓W_0の4個の画素O_{00}、O_{01}、O_{10}、O_{11}の画像信号レベルを出力とする順位付用記憶手段、5は順位付用記憶手段4の出力信号である走査窓W_0の4個の画素O_{00}、O_{01}、O_{10}、O_{11}の画像信号レベルと後述する順位付補正手段の出力である近傍補正量Ebを入力とし、4個の画素の画像信号レベルの比較により画素順位を決定しそれを出力とする順位決定手段である。6は再配分演算手段3の出力信号である配分数N（又はN＋1）と順位決定手段5の出力手段である画素順位とを入力として、画素順位に応じて前記配分数N（又はN＋1）と走査窓Wrの4画素数とを比較し、N（又はN＋1）＜4個のとき、所定の画像信号レベルCnと0との配分を、又、N（又はN＋1）＝4個のとき所定の画像信号レベルCnを配分し、また、N（又はN＋1）＞4個のとき、所定の画像信号レベルCnを画素順位に応じてM個配分し、更に再び〔N（又はN＋1）〕個の画像信号レベルCnを先の順位に応じて割当てた画像信号レベルCnに加算して決定した結果を再配分用画像信号レベルとして出力する再配分手段、7は配分値演算手段6の出力である総和Sと残差Aと配分数N（又はN＋1）を入力して配分誤差e_nを演算し出力する配分誤差演算手段、8はW_0の画素O_{00}の画像信号レベルと再配分用記憶手段2の出力信号である再配分済画素R_{00}の多値化画像信号レベルと後述する補正量記憶手段の出力信号である順位付補正量Ecとを入力とし後述する演算により近傍補正量Ebと新たな順位付補正量Ecとを出力とする順位付補正手段、9は既に記憶してある順位付補正量Ecを出力とし順位付補正手段8の出力信号である新たな順位付補正量Ecを記憶する補正量記憶手段、10は再配分用記憶手段2の出力信号である再配分済画素R_{00}の多値化画像信号レベルを入力して多値画像を記録又は表示する画像記録・表示手段である。

第2図は本実施例の具体的な回路図で第1図で示す画像信号処理装置のブロック図の構成の主要部である再配分用記憶手段2〜補正量記憶手段9をマイクロコンピュータで実現したものである。第2図において、11は原画像走査手段1の出力信号である原画像の画像信号レベルを入力する入力端子である。インプットポート12はゲートより構成されており、CPU13より信号線14を介して与えられる選択信号により入力端子11からの画像信号レベルをCPU13へ出力する。ROM15にはCPU13を制御するプログラムが込められており、CPU13はこのプログラムに従ってインプットポート12より必要とされる外部データを取込んだり、あるいはRAM16との間でデータの授受を行なったりしながら演算処理し、必要に応じて処理したデータをアウトプットポート17へ出力する。アウトプットポート17はラッチ回路より構成されており、信号線18を介してアウトプットポート17へ与えられるCPU13からの出力

ポート指定信号を受けて、そのポートにデータを一時記憶する。19はアウトプットポート17に一時記憶されているデータを多値化した画像信号レベルとして画像信号記録・表示手段10へ出力する出力端子である。

なお、CPU13、ROM15、RAM16は周知のマイクロコンピュータにより構成することができる。

ROM15に書きこまれているプログラムをフローチャートで示すと第3図のようになる。以下第3図に従って第1図に示した画像信号処理装置の動作を説明する。

プログラムがスタートすると、まず再配分用記憶手段2、順位付用記憶手段4、補正量記憶手段9、配分誤差演算手段10の内容を0クリアし初期設定を行う。（ステップ1）

次に原画像信号を再配分用記憶手段2の走査窓Wrの画素R_{11}と順位付け記憶手段4の走査窓W_0の画素0_{11}に読み込む（ステップ2）。

次に再配分用記憶手段2の走査窓Wr内の4個の画素R_{00}、R_{01}、R_{10}、R_{11}の画像信号レベル加算値Smと、一画素前に発生した配分誤差e_nとの和S（$=Sm+e_n$）を演算する。次に画像信号の最大値Cを記録・表示できる濃度レベル数n−1で除算した画像信号レベルCnを求め、和$S=Cn×N+A$となる画像信号レベルCnの配分数Nと残差Aを演算し、更に画像信号レベルCnの半値画像信号レベルCn/2と残差Aとを比較して残差Aが$A≧Cn/2$のとき画像信号Cnの配分数をN+1とし、残差Aが$A<Cn/2$のとき、配分数をNとする。（ステップ3）。

次に補正量記憶手段9の走査窓Wc内の順位付補正量記憶位置Ec_1、Ec_2、Ec_5、Ec_4、の4個の順位付補正量Ecの平均値Ecaと係数Kaから近傍補正量Eb（$=Ka×Eca$）を演算する（ステップ4）。

次に順位付用記憶手段4の走査窓W_0の画素0_{00}の画像信号レベルに近傍補正量Ebを加算した後、4個の画素0_{00}、0_{01}、0_{10}、0_{11}の画像信号レベルをそれぞれ比較し大きい順に画素順位を決定する（ステップ5）。

次にステップ3で求めた配分数N（又はN+1）がN（又はN+1）＜4のとき、ステップ5で求めた画素順位に従って画像信号レベルCnと0を再配用記憶手段2の走査窓Wrの4個の画素R_{00}、R_{01}、R_{10}、R_{11}の画像信号レベルとし、又N（又はN+1）＝4のときはCnを走査窓Wrの4個の画素R_{00}、R_{01}、R_{10}、R_{11}の画像信号レベルとする。また配分数N（又はN+1）がN（又はN+1）＞4のとき、すでに画素順位に従って配分した画像信号レベルCnに〔N（又はN+1）〕個の画像信号レベルCnを再びステップ5で求めた画素順位に従って加算して決定した結果を再配分用記憶手段2の走査窓Wrの4個の画素R_{00}、R_{01}、R_{10}、R_{11}の画像信号レベルとし、そして再配分済画素R_{00}を多値化画像信号レベルとする（ステップ6）。

次にステップ3で求めた総和Sと、画像信号レベルCnの

配分数N（又はN+1）と、残差Aから配分誤差enを次のように求める。配分数がN+1のとき、配分誤差en（$=S−(Cn×(N+1))$）配分数がNのとき、配分誤差e_n（$=A$）なる演算し一時レジスタに記憶する。（ステップ7）。

次にステップ4における平均値Ecaと係数Kbを集算した値に走査窓W_0内の画素0_{00}の画像信号レベルを加算し、その値とステップ6における再配分済画素R_{00}の多値化画像信号レベルとの差分を新たな順位付補正量Ecとし走査窓We内の画素Ec_5に記憶する（ステップ8）。

次にステップ6で求めた再配分済画素R_{00}の多値化画像信号レベルを画像記録・表示手段10へ出力する（ステップ9）。

次にすべての原画像信号レベルに対して主走査方向および副走査方向の処理終了判定をし（ステップ10）、未終了であれば走査窓の移動を行い（ステップ11）ステップ2より繰返す。もし終了であれば全原画像信号に対して処理を完了する。ただし、主走査方向の処理が終了する毎にステップ11において配分誤差e_nを0クリアする。

なお上記説明ではマイクロコンピュータにより再配分記憶手段2〜補正量記憶手段9を実現したが、これらの手段はそれぞれ論理回路、外部メモリ等により実現することもできる。

さらに順位付補正手段8の係数Kaは$1/2^L$（ただし、Lは正の整数）にすることにより、また係数Kbは$1−1/2^m$（ただし、mは正の整数）にすることによりマイクロコンピュータで実現した場合には演算を容易にすることができ、論理回路で実現した場合にはハードウエアを軽減することができる。

発明の効果

以上のように本発明によれば画像信号の最大値Cをnレベルの出力階調数n−1で除算した画像信号レベルCnを配分値とし、総和Sから得られるCnの配分数Nと残差Aを求め、その残差Aを半値画像信号レベルCn/2と比較して、Cnの配分数を制御し、配分誤差e_nを小さくすることによって、滑らかな再生画像を得ることができる。

【図面の簡単な説明】

第1図は本発明の一実施例における画像信号処理装置のブロック結線図、第2図は同装置をマイクロコンピュータで実現した具体的な回路図、第3図は本実施例の動作を説明するフローチャート、第4図は従来の多値組織ディザ法を実現する装置のブロック結線図である。

1…原画像走査手段、2…再配分用記憶手段、3…配分値演算手段、4…順位付用記憶手段、5…順位決定手段、6…再配分手段、7…配分誤差演算手段、8…順位付補正手段、9…補正量記憶手段、10…画像記録・表示手段、11…入力端子、12…インプットポート、13…CPU、14,18…信号線、15…ROM、16…RAM、17…アウトプットポート、19…出力端子。

【第1図】

【第2図】

原画像の
画像信号レベル → インプットポート (12) → CPU (13) → アウトプットポート (17) → 多値化した画像信号レベル

RAM (16)

ROM (15)

11 12 14 16 13 15 17 18 19

【第3図】

```
                        ┌──────┐
                        │ 開 始 │
                        └──┬───┘
                           ↓
ステップ1          ┌──────────┐
                  │ 初 期 設 定 │
                  └────┬─────┘
                       ↓←──────────────────────┐
ステップ2          ┌──────────┐                │
                  │画像信号の読込み│                │
                  └────┬─────┘                │
                       ↓                      │
ステップ3      ┌────────────────┐            │
              │配分数Nと残差Aの演算│            │
              │から新たな配分数の演算│            │
              └────────┬───────┘            │
                       ↓                      │
ステップ4      ┌────────────────┐            │
              │近傍補正量Ebの演算│            │
              └────────┬───────┘            │
                       ↓                      │
ステップ5          ┌──────────┐                │
                  │画素順位決定│                │
                  └────┬─────┘                │
                       ↓                      │
ステップ6      ┌────────────────┐            │
              │画素順位にN個の  │            │
              │Cnを再配分      │            │
              └────────┬───────┘            │
                       ↓                      │
ステップ7      ┌────────────────┐            │
              │配分誤差の演算    │            │
              └────────┬───────┘            │
                       ↓                      │
ステップ8      ┌────────────────┐            │
              │新たな順位付補正量 │            │
              │Ec を求める     │            │
              └────────┬───────┘            │
                       ↓                      │
ステップ9      ┌────────────────┐            │
              │多値化画像信号の出力│            │
              └────────┬───────┘            │
                       ↓                      │
ステップ10       ◇走査終了?◇──NO──→ ステップ11 ┌──────────┐
                       │                      │走査窓の移動│──┘
                      YES                     └──────────┘
                       ↓
                   ┌──────┐
                   │ 終 了 │
                   └──────┘
```
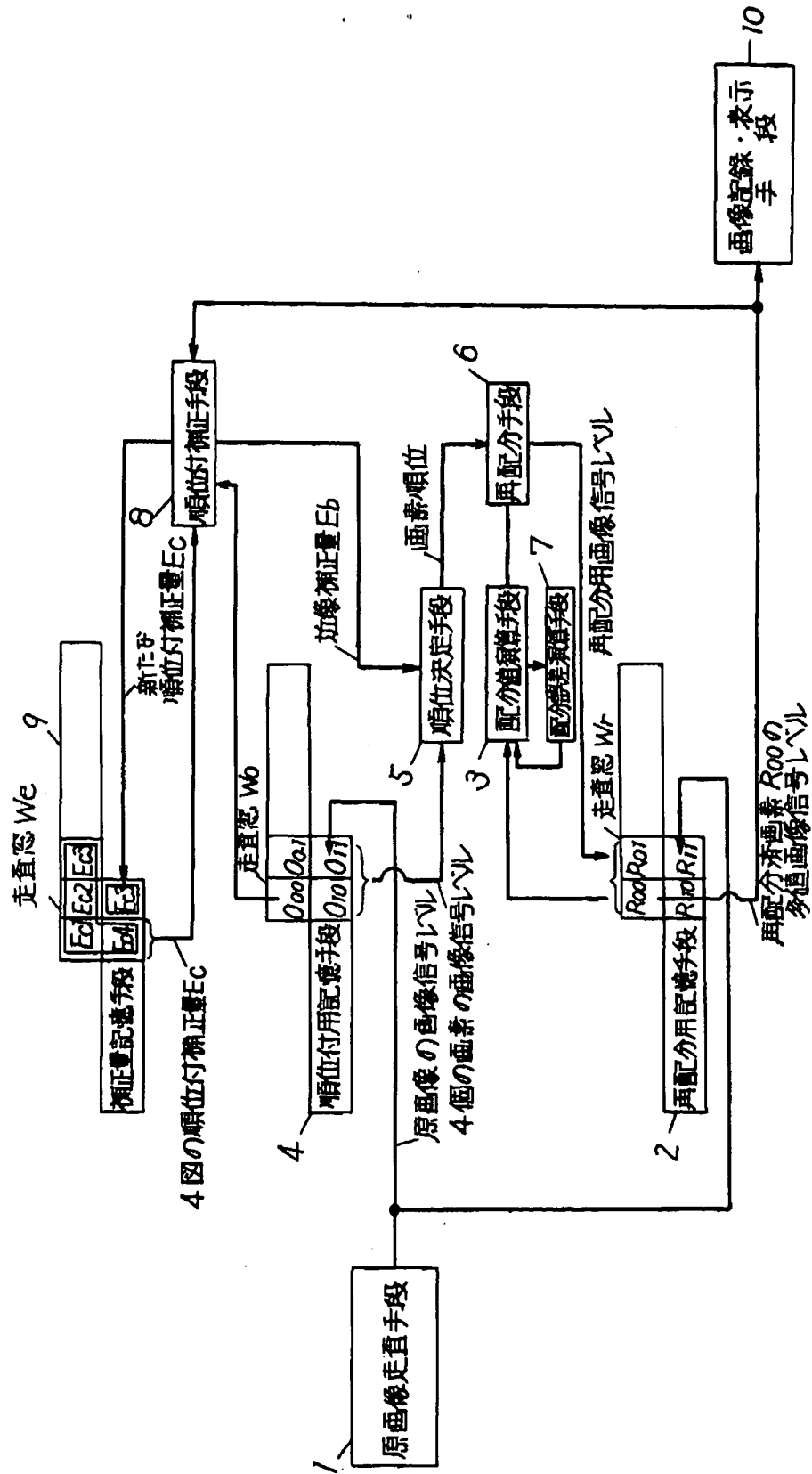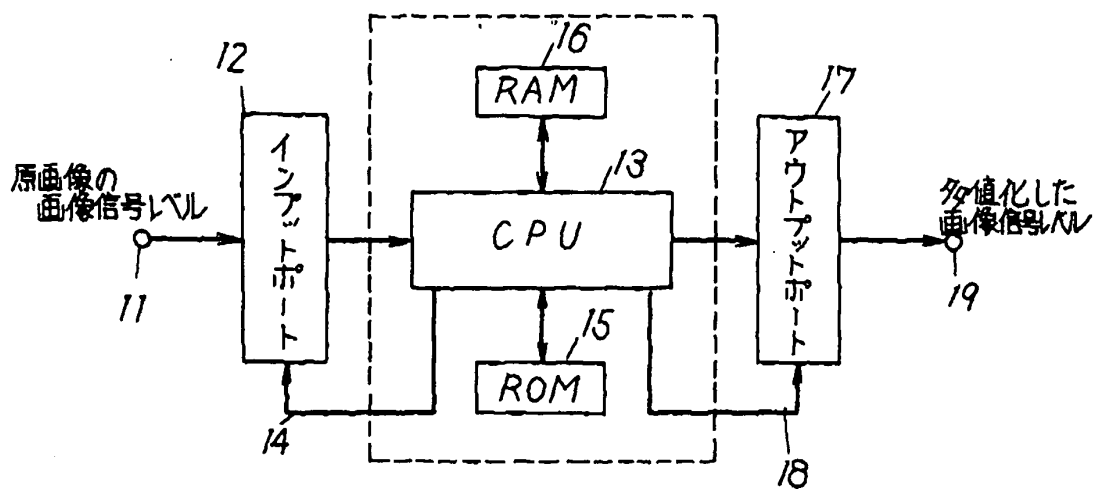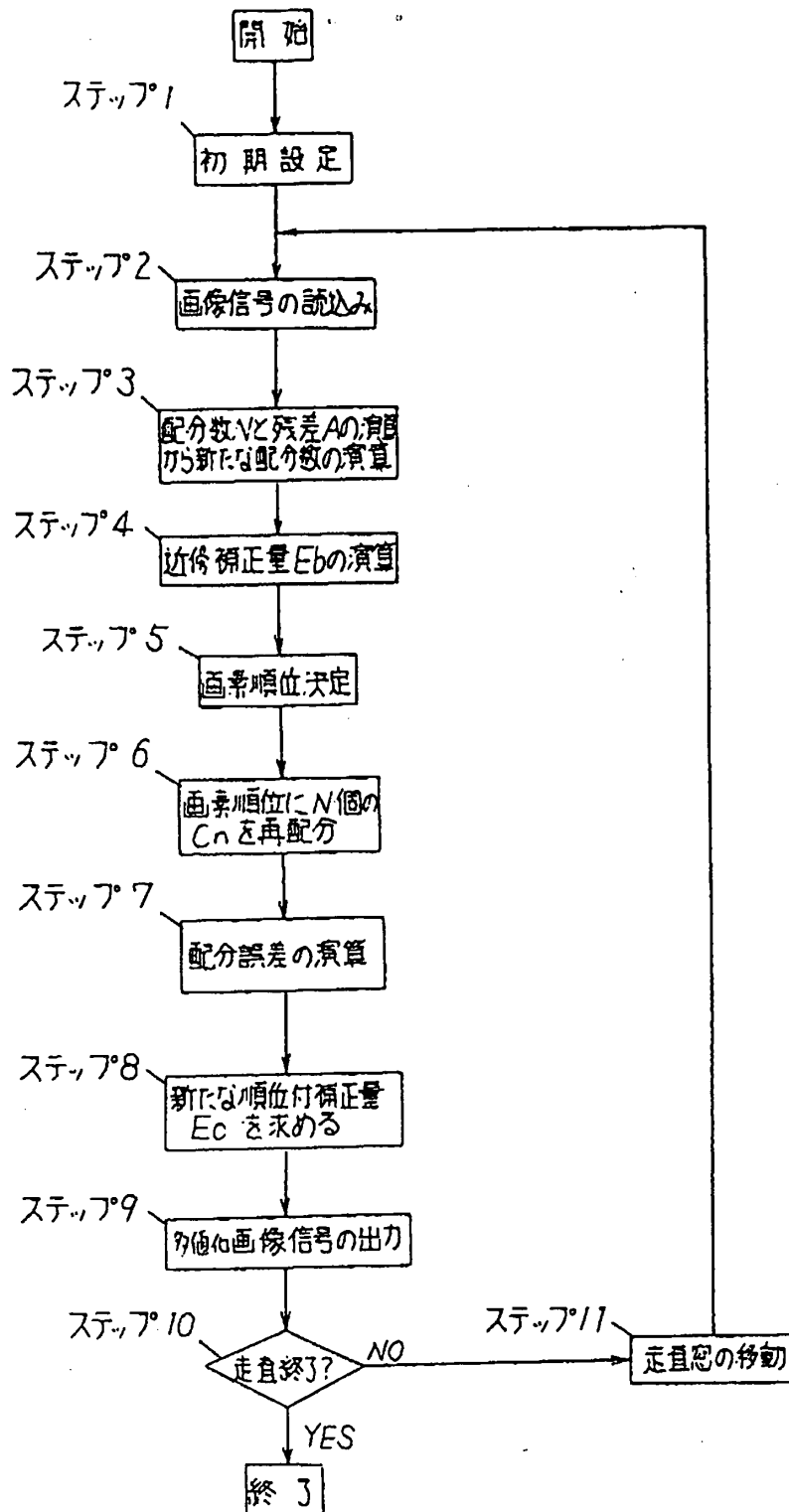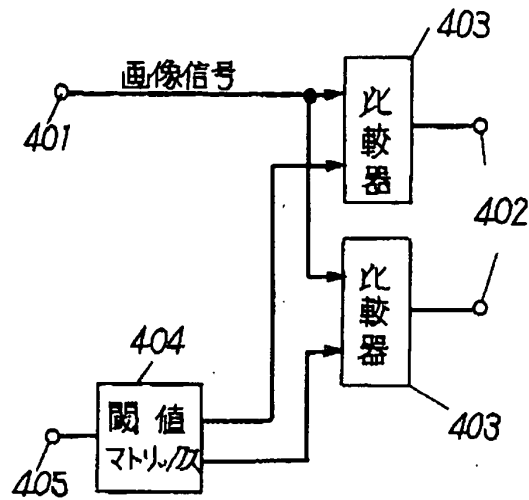
【第4図】

(a)

(b)

14	30	10	26	6	22	15	31
5	21	1	17	2	18	11	27
9	25	4	20	3	19	7	23
13	29	8	24	12	28	16	32

(C)

比較器の出力		記憶レベル
0	0	0
0	1	1/2
1	0	
1	1	1

出　願　758,961　　　　(1985. 7.25)

原出願

特　許　4,692,811　　　(1987. 9. 8)

原特許

名　称　Apparatus for processing image signal

抄　録　The invention relates to a method for processing an image signal such
that areas of original image data are sequentially scanned with a scanning
window having a size corresponding to M picture elements in units of a
predetermined number of picture elements so as to perform halftone display in
accordance with black-and-white binary distribution with respect to the signal
levels of the picture elements within the scanning window every time the
scanning window is moved. The picture elements within the scanning window are
assigned an order of preference in accordance with their image signal levels. A
sum of the image signal levels of the picture elements within the scanning
window is calculated, and A and N of the equations $S = C \text{.times.} N + A$ are calculated,
where C is a predetermined image signal level (e.g., black level and maximum
level), N is an integer, and A is the image signal level falling within the
range $0.1 \text{toreq.} A < C$. As a result of the preference operation, N picture elements
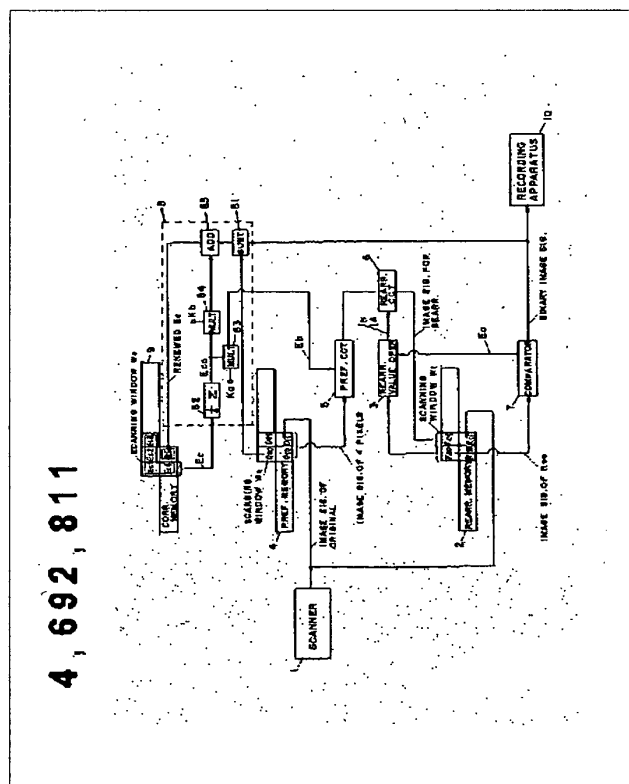are assigned a level C

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【米国引例特許】4,491,963 01/1985 Bellemare 358282
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【要約】

<ABSTRACT>
The invention relates to a method for processing an image signal such that areas of original image data are sequentially
scanned with a scanning window having a size corresponding to M picture elements in units of a predetermined number of
picture elements so as to perform halftone display in accordance with black-and-white binary distribution with respect to
the signal levels of the picture elements within the scanning window every time the scanning window is moved. The picture
elements within the scanning window are assigned an order of preference in accordance with their image signal levels. A
sum of the image signal levels of the picture elements within the scanning window is calculated, and A and N of the
equations $S=C.times.N+A$ are calculated, where C is a predetermined image signal level (e.g., black level and maximum
level), N is an integer, and A is the image signal level falling within the range $0.1toreq.A<C$. As a result of the
preference operation, N picture elements are assigned a level C, the next picture element is assigned a level A, and the
remaining picture elements, 0. In order to impart regularity to the converted image signal distribution, additional data
is added to the preference data.
【発明概要】
<BACKGROUND OF THE INVENTION>
The present invention relates to an apparatus for processing an image signal having functions of halftone image
reproduction in binary.
Recently, facsimile systems have become frequently used in daily business. There arises a demand for halftone reproduction
of pictorial images in addition to back-and-white binary reproduction of documents or the like. However, halftone
reproduction often has many restrictions from the viewpoints of recording apparatuses and transmission systems. For
example, an apparatus for recording an image on a silver chloride film used in conventional photography or a
heat-sensitive printing apparatus has good recording characteristics for halftone recording. However, an electrostatic
copying machine or an ink jet printing apparatus has good characteristics for binary recording. On the other hand,
regarding transmission systems, digital data transmission is taking over from analog data transmission. In this field,
data compression schemes are used to perform high-speed data transmission. Under these conditions, a pseudo halftone
display system having a binary recording apparatus is proposed, which is suitable for digital data transmission, thereby
providing an optimum fascimile system.
An electronic halftone-dot generating method for a printed image in a newspaper or magazine and a dither method for
digitizing or quantizing an image signal in accordance with a threshold matrix table are typical examples of a pseudo
halftone display system. However, these conventional methods have poor resolution of a two-valued (binary) image such as a
character or line. Therefore, the halftone portion or binary image portion cannot help but be sacrificed.
For example, according to the dither method, in a threshold window consisting of a threshold pattern of a plurality of
different threshold levels, a multilevel input image signal is compared with the threshold levels in units of picture
elements. When a given picture element level of the original image data exceeds the corresponding threshold, the picture

element is set to "black". Otherwise, the picture element is set to "white". In this manner, each picture element is converted to binary data. When a 4.times.4 matrix window is used, 16 threshold levels can be set. Therefore, halftone display having 17 levels can be performed for the original image data. In this manner, according to the conventional dither method, black elements appear in each threshold window in a number corresponding to the original image data levels, so as to represent an average halftone mode. When the window size is small, the displayed image has good resolution. In this case, however, the number of halftone levels is decreased. On the other hand, if the window size is large, the number of halftone levels is increased. However, in this case; resolution is degraded. In addition to this disadvantage, the quality of a reproduced image of a binary original image portion is degraded in accordance with the conventional dither method, as compared with general binary processing.

Some of inventors of this application previously invented an apparatus and a method for converting halftone image signals into binary signals. The method is now patent pending in United States and other countries (U.S. patent Ser. No. 501,873, now U.S. Pat. No. 4,538,184; British patent publication No. 2,129,652, etc.) The method comprises defining a successively shifted scanning window with respect to the signal level of each picture element from which said video signal has been derived, totalizing the quantum numbers of the picture elements in the scanning window corresponding to the original screen dot, and reconstructing black picture elements corresponding to the total value of the quantum numbers faithfully to the area of the original dot. This method realizes binary data reproduction with no moire pattern, but it is not sufficient to obtain both of high resolution and multiple halftone levels.

<SUMMARY OF THE INVENTION>

It is, therefore, an object of the present invention to provide an apparatus for processing an image signal so as to provide a displayed/recorded image of good image quality for both a binary image and a halftone image.

It is another object of the present invention to provide an apparatus for processing an image signal to obtain pseudo halftone reproduction compatible with both of high resolution and multiple halftone levels.

According to the present invention, there is provided an apparatus for processing an image signal comprising,

first and second image signal memory means for storing image signal levels of picture elements which are obtained by scanning an original image in a divided manner;

means for calculating a sum S of error correction data E.sub.a and a sum S.sub.m of the image signal levels of all picture elements within a first scanning window which a has a size corresponding to M picture elements and which scans said first image signal memory means, and obtaining N and A from equation

S=C.times.N+A

where C is a predetermined image signal level, N is an integer falling in a range 0.ltoreq.N.ltoreq.M, and A is an image signal level falling in a range 0.ltoreq.A.ltoreq.C;

preference circuit means for numbering all picture elements to one of which neighboured correction data E.sub.b is added, within a second scanning window which has a size corresponding to M picture elements so as to scan said second image signal memory means, in accordance with one of ascending and descending orders of the image signal levels;

rearrangement circuit means for assigning C as an image signal level to N picture elements of M picture elements in said first image signal memory means ordered by said preference circuit, A as an image signal level to a next picture element, and 0 as an image signal level to remaining picture elements,

means for comparing an image signal level of rearranged picture element with a predetermined quantizing level V for 0.ltoreq.V<, and for assigning C to the image signal level when the image signal level is greater than the quantizing level V as a binary image signal and assigning 0 to the image signal level when the image signal level is smaller than the quantizing level V as another binary image signal, and oprating the error correction data E.sub.a from the difference of the image signal level and the assigned binary image signal,

third memory means for storing preference correction data,

a first calculating means for calculating the neiboured correction data E.sub.b by the preference correction data neiboured to the refered picture element corresponding to that in said first or second scanning window and,

a second calculating means for calculating renewed preference correction data which are to be stored into address corresponding to the refered picture element with the preference correction data read out from said third memory, image signal level of the refered picture element in said second image signal memory, and the binary image signal level.

【図面の簡単な説明】

<BRIEF DESCRIPTION OF THE DRAWINGS>

The present invention will now be described in further detail with reference to the accompanying drawings, in which:

FIG. 1 is a block diagram of an image signal processing apparatus of the first embodiment of the present invention;

FIG. 2 is a block diagram of the preference circuit of FIG. 1;

FIG. 3 is a flow chart for explaining processing steps of the embodiment of FIG. 1;

FIG. 4 is a block diagram of an image signal processing apparatus of the second embodiment of the present invention;

FIG. 5 is a flow chart for explaining processing steps of the embodiment of FIG. 4;

FIG. 6 is a block diagram of an image signal processing apparatus of the third embodiment of the present invention;

FIG. 7 is a flow chart for explaining processing steps of the embodiment of FIG. 6;

FIG. 8 is a block diagram of an image signal processing apparatus of the fourth embodiment of the present invention;

FIG. 9 is a flow chart for explaining processing steps of the embodiment of FIG. 8;

FIG. 10 is a block diagram of an image signal processing apparatus of the fifth embodiment of the present invention;

FIG. 11 is a flow chart for explaining processing steps of the embodiment of FIG. 10;

FIG. 12 is a block diagram of an image signal processing apparatus of the sixth embodiment of the present invention;

FIG. 13 is a flow chart for explaining processing steps of the embodiment of FIG. 12; and

FIG. 14 is a block diagram of an image signal processing apparatus of the seventh embodiment of the present invention.

【発明の詳細な説明】

〈DETAILED DESCRIPTION OF THE INVENTION〉

Through this specification and drawings, size M of the scanning windows is fixed to 4. The picture element addresses in the first scanning window are denoted with symbols $R.sub.00$, $R.sub.01$, $R.sub.10$ and $R.sub.11$. Similarly, the picture element addresses in the second scanning window are denoted with symbols $O.sub.00$, $O.sub.01$, $O.sub.10$ and $O.sub.11$. In the third memory, the refered address is denoted with symbol $E.sub.c5$, and the neighboured addresses are $E.sub.c1$, $E.sub.c2$, $E.sub.c3$ and $E.sub.c4$. The picture element addresses $R.sub.00$, $O.sub.00$ and the address $E.sub.c5$ are corresponded to same picture element in referring. Defined $R.sub.00$, $R.sub.01$, $R.sub.10$ and $R.sub.11$ as a scanning window $W.sub.r$, $O.sub.00$, $O.sub.01$, $O.sub.10$ and $O.sub.11$ as a scanning window $W.sub.0$, and $E.sub.c1$, $E.sub.c2$, $E.sub.c3$, $E.sub.c4$ and $E.sub.c5$ as a scanning window $W.sub.e$ respectively. The scanning windows $W.sub.r$, $W.sub.o$ and $W.sub.e$ are shifted right in synchronism with main scan of scanner 1.

FIG. 1 illustrates the first embodiment of the present invention. In FIG. 1, numeral 1 denotes a scanner which scans original and outputs image signal level as digital signal. The scanner 1 is almost same as those disclosed in U.S. patent application Ser. No. 501,873 or British patent publication No. 2,129,652. The output signal from the scanner is supplied to a rearrangement memory 2 and a preference memory 4. The rearrangement memory 2 stores the output signal from the scanner 1 and output signal from a data rearrangement circuit 6 and outputs image signal levels of four picture elements $R.sub.00$, $R.sub.01$, $R.sub.10$ and $R.sub.11$ in the scanning window $W.sub.r$. A rearrangement volue operator 3 calculates a sum S of an error correction data $E.sub.a$ from a comparator 7 and a sum $S.sub.m$ of the image signal levels of four picture elements $R.sub.00$, $R.sub.01$, $R.sub.10$ and $R.sub.11$ from the rearrangement memory 2, and obtaining N and A from following equation $S=C.times.N+A$, where C is a predetermined image signal level, N is an integer falling in a range $0.ltoreq.N.ltoreq.M$, and A is an image signal level falling in a range $0.ltoreq.A.ltoreq.C$. The preference memory 4 receives image signal of original from the scanner and outputs image signal levels of four picture elements $O.sub.00$, $O.sub.01$, $O.sub.10$ and $O.sub.11$ in the scanning window $W.sub.o$. The image signal levels from the preference memory 4 are supplied to a preference circuit 5 to which neighboured correction data $E.sub.b$ is supplied from a multiplier 83. The preference circuit determines preference order of the four picture elements by comparing image signal levels of the four picture elements, to $O.sub.00$ picture element of which neighboured correction data $E.sub.b$ is added from a multiplier 83, in accordance with one of ascending and descending orders of the image signal levels. A data rearrangement circuit 6 receives data N and A from the preference value operator 3 and assign C as an image signal level to N picture elements of four picture elements in the scanning window $W.sub.r$ in order determined by the preference circuit 5, A as an image signal level to a next picture element, and 0 as an image signal level to remaining picture element. Numeral 7 denotes a comparator which compares image signal of rearranged picture element $R.sub.00$ from the rearrangement memory 16 with a predetermined quantitizing level V, where $0.ltoreq.V<C$, and outputs C as image signal level to be recorded or displayed when the image signal $R.sub.00$ is greater than the level V, and outputs 0 as image signal level to be recorded or displayed when the image signal $R.sub.00$ is smaller than the level V. At the same time, the comparator 7 outputs error correction data $E.sub.a$ which is the difference between the image signal $R.sub.00$ and the output signal of the comparator 7. Numberal 8 designates a preference correction means which receives image signal level of the picture element $O.sub.00$ from the preference memory 4, output image signal level of the comparator 7, and preference correction data $E.sub.c$ from a correction data memory 9 and operates neighboured correction data $E.sub.b$ and preference correction data $E.sub.c$ to be renewed. The renewed correction data $E.sub.c$ are stored into address $E.sub.c5$ of the correction data memory 9. The output signal from the comparator 7 is supplied to a recording or display apperatus 10 to record or display binary image. The apparatus 10 may be same as that disclosed in U.S. patent application Ser. No. 501,873.

The preference correction means 8 comprises a subtracter 81 for subtracting output signal level of the comparator 7 from the image signal level of the picture element $O.sub.00$ in the scanning window $W.sub.o$, an average operator 82 for

calculating average E_{ca} of four preference correction data E_{c1}, E_{c2}, E_{c3} and E_{c4} in the scanning window W_e, a first multiplier 83 for multiplying a predetermined coefficient K_a to the average E_{ca}, a second multiplier 84 for multiplying a predetermined coefficient K_b to the average E_{ca}, and an adder 85 for adding the output of the multiplier 84 and the output of the subtracter 81.

In FIG. 1, the constructions and operations of the scanner 1, the rearrangement memory 2, the rearrangement value operator 3, the preference memory 4, the preference circuit 5, the data rearrangement circuit 6, the comparator 7 and the recording or display apparatus 10 are substantially same as those of U.S. patent application Ser. No. 501,873 or British patent publication No. 2,129,652.

FIG. 2 illustrates a block diagram which realizes the part including from the rearrangement memory 2 to the correction data memory 9 of FIG. 1 with a microcomputer. Image signal level of original obtained from the scanner 1 is supplied to an input terminal 11. Input port 12 is a gate circuit which supplies image signal level from the input terminal 11 to CPU13 (central processing unit) in accordance with a selective signal given from the CPU13 through a signal line 14. ROM 15 (read only memory) stores a program for controlling the CPU13. In accordance with the program, the CPU takes in necessary data from the input port 12, performs predetermined operations by giving and taking data between RAM16 (random access memory), and supplies output data to output port 17. The output port 17 is a latch circuit which stores data temporarily in accordance with a control signal given from the CPU 13 through a signal line 18. The data stored in the output port 17 are took out to an output terminal 19 as a binary image signal to be recorded or displayed.

The CPU13, ROM15 and RAM16 can be constructed by wellknown microcomputer.

FIG. 3 illustrates a flow chart corresponding to the program stored in the ROM15.

When the program starts, the contents of the rearrangement memory 2, the preference memory 4 and the correction data memory 9 and error correction data E_a are cleared (STEP 1). In STEP 2, the image signal of the original is written into the address of picture element R_{11} of the rearrangement memory 2 and the address of picture element O_{11} of the preference memory 4. In STEP 3, the rearrangement value operator 3 calculates a sum S of the error correction data E_a and a sum S_m of the image signal levels of picture elements R_{00}, R_{01}, R_{10} and R_{11} within the scanning window W_r of the rearrangement memory 2, and operates integer N and remainder A from equation $S = C \times N + A$. In STEP 4, the average operator 82 calculates an average E_{ca} of four preference correction data E_{c1}, E_{c2}, E_{c3}, and E_{c4} within the scanning window W_e of the correction data memory 9, and the average E_{ca} is multiplied by the predetermined coefficient K_a in the multiplier 83 to obtain neighboured correction data E_b ($= K_a \times E_{ca}$). The coefficient K_a is, for example, $1/2^n$, where n is an integer. In STEP 5, the preference circuit 5 adds the neighboured correction data E_b to the image signal level of the picture element O_{00} within the scanning window W_o of the preference memory 4, and determines rearranging order of four picture elements O_{00}, O_{01}, O_{10}, and O_{11} in descending order by comparing the image signal levels thereof. In step 6, the data rearrangement circuit 6 rearranges N predetermined image signal level C, the remainder A and 0 which are obtained in STEP 3, as image signals of four picture elements R_{00}, R_{01}, R_{10} and R_{11} within the scanning window W_r of the rearrangement memory 2 according to the order obtained in STEP 5. In STEP 7, the comparator 7 converts the image signal of the rearranged picture element R_{00} from the rearrangement memory 2 into binary image signal with the quantitizing level V, and the difference between the image signal of the picture element R_{00} and the converted binary signal is supplied to the rearrangement volue operator 3 as a renewed error correction data E_a for next STEP 3. In STEP 8, the preference correction means 8 calculates the product of the coefficient K_b and the average E_{ca} obtained in STEP 4 by the multiplier 84, and adds the product to the difference between image signal level of the picture element O_{00} in the scanning window W_o and the binary image signal level from the comparator 7, which is calculated by the subtracter 81, in the adder 85 to produce renewed preference correction data E_c which is to be stored in the picture element E_{c5} within the scanning window W_e of the correction data memory 9. In STEP 9, the binary image signal from the comparator 7 is supplied to the display apparatus 10. In STEP 10, it is judged whether the above processes are ended relating to all of image signals of original in both of main and sub scans. If the processes are not ended, the scanning windows W_o, W_r and W_e are moved and the STEP 2 to STEP 10 are repeated. In this case, the error correction data E_a is cleared in every end of main scans in STEP 11.

When the coefficient K_a is $1/2^n$ and K_b is 114 $1/2^m$, where n and m are positive integers, the operations in the microcomputer become easy.

The microcompter may be replaciable with logic circuits and memories. In this case, hardware thereof can be simplified by using the above valued coefficients K_a and K_b.

FIG. 4 illustrates another embodiment of the present invention. In Fig. a signal adder 20 is provided between the canner 1 and the preference memory 4. The signal adder 20 adds a periodical signal in synchronism with the picture elements of the

original image and having different signal level thereof to the original image signal forn the scanner 1. The signal adder 20 is substantially same as that shown in British patent publication No. 2,129,652. Other portions of FIG. 4 are same as those of FIG.'1. In this embodiment, the periodical signal is supperposed to the original image signal as STEP 2 shown in FIG. 5. The remaining steps are same as those in FIG. 3. The embodiment improves visual characteristics of the reproduced image with diverging error data in the additive signal. When a random signal is superposed as the additive signal, the improvement of moire signal or reproduction of image having special effect are obtained.

FIG. 6 illustrates a third embodiment of the present invention. A compensator 21 is provided between the comparator 7 and the recording or display apparatus 10. The compensator 21 selects the binary image signal from the comparator 7 in accordance with the image signal level of the picture element O_{00} within the scanning window W_o of the preference memory 4. Other portions of FIG. 6 are same as those of FIG. 1.

In the operation shown in FIG. 7, STEP 9 is newly added after renewing E_c in STEP 8, which corresponding to STEP 8 of FIG. 3. In STEP 9 of FIG. 7, the compensator 21 compares the image signal level of the picture element O_{00} in the scanning window W_o of the preference memory 4 with predetermined low level value Tl and high level volue Th, and selects onput signal level as below.

(1) Output 0 when O_{00} .ltoreq.Tl;

(2) Output C when O_{00} .gtoreq.Th;

(3) Output the binary image signal from the comparator 7 when $Tl < O_{00} < Th$;

where O_{00} is the image signal level of the picture element O_{00}, and C is a predetermined recording level, which usually corresponds to maximum recording level. The embodiment suppresses noises contained in high and low level of the binary image signal.

FIG. 8 illustrates 9 fourth embodiment of the present invention. In FIG. 8, the constructions and/or connections of the rearrangement memory 22, the rearrangement volue operator 23 and the data rearrangement circuit 26 are different from those of FIG. 1. Other portions are same as those of FIG. 1. The rearrangement memory 22 receives rearrangement image signal level from the data rearrangement circuit 26, and stores upper U bit of the rearrangement image signal level in three picture element R_{00}, R_{01}, and R_{10} within the scanning window W_r, and supplies the stored upper U bit signal to the rearrangement value operator 23. The rearrangement value operator 23 calculates a sum S of a volue Su which is obtained by inserting 0 to each of lower L bit of a sum of the three image signal levels of the picture elements R_{00}, R_{01}, and R_{10} from the rearrangement memory 22, error correction data E_a from the comparator 7, image signal level F_o of the original from the scanner 1, and rearrangement correction data S, from the data rearrangement circuit 26, and obtaining N and A from $S = C.times.N + A$ similierly to the case of FIG. 1. The data rearrangement circuit 26 comprises means for determining arrangement of C for N picture elements, A and 0 for remaining picture elements in accordance with the preference order designated by the preference circuit 5, means for storing upper U bits data of the image signal levels for rearrangement into three picture elements R_{01}, R_{10}, and R_{11} within the scanning window W_r of the rearrangement memory 22, means for obtaining the renewed rearrangement correction data S_l by summing lower L bits data of the image signal levels for rearrangement and means for supplying all bits data of the image signal levels corresponding to the picture element R_{00} within the scanning window W_r of the rearrangement memory 22 to the comparator 7.

FIG. 9 illustrates a flow chart for explaining operations of the block diagram of FIG. 8.

When the program starts, the contents of the rearrangement memory 22, the preference memory 4 and the correction data memory 9, and error correction data E_a and rearrangement correction data S_l are cleared (STEP 1). In STEP 2, the image signal level F_o of the original is written into the rearrangement value operator 23 and the address of picture element O_{11} within the scanning window W_o of the preference memory 4. In STEP 3, the rearrangement value operator 23 calculates the sum S ($= Su + Ea + S_l + F_o$) and operates integer N and remainder A from equation $S = C.times.N + A$. STEP 4 and STEP 5 are similar to those of FIG. 3. In STEP 6, the upper U bits data of the image signal levels for rearrangement C, A and 0 into three picture elements R_{01}, R_{10} and R_{11} within the scanning window W_r of the rearrangement memory 22 in accordance with the preference order obtained in STEP 5, the sum of lower L bits data of the image signal levels in the three picture elements R_{01}, R_{10}, R_{11}, within the scanning window W_r is supplied to the rearrangement value operator 23 as renewed rearrangement correction data S_l and all bits data of the image signal levels of the rearranged picture element R_{00} are supplied to the comparator 7. These are performed by the data rearrangement circuit 26. STEP 7 to STEP 11 are similar to those of FIG. 3. The embodiment saves the amount of buffer memory used as the rearrangement memory 22 from U+L bits to U bits.

FIG. 10 illustrates a fifth embodiment of the present invention. The correction data memory 29 is smaller in bit number (U bit) than that (U+L bit) of the correction data memory 9 of FIG. 1. To compensate this, a lower bit gate 86, an upper bit gate 87 and an adder 88 are provided in the preference correction means 8. Other portions are same as those of FIG. 1.

FIG. 11 illustrates a flow chart for explaining operations of the block diagram of FIG. 10.

When the program starts, the contents of the rearrangement memory 2, the preference memory 4 and the correction data memory 9, and error correction data E_a, preference correction data E_{ca} from the adder 88, upper bit preference correction data E_{cu} from the gate 87, and lower bit preference correction data E_{CL} are cleared (STEP 1). STEP 2 and STEP 3 are same as those of FIG. 3. In STEP 4, the average operator 82 calculates average of four preference correction data which are formed with four upper bit preference correction data E_{CU} having U bits from addresses E_{c1}, E_{c2}, E_{c3} and E_{c4} within the scanning window W_e of the correction data memory and 0 inserted to lower L bit thereof, and the adder 88 adds the average from the average operator 82 and the lower bit preference correction data E_{CL} selected by the gate 86 and delayed in time corresponding to one picture element. The thus obtained sum E_{ca} is multiplied by a coefficient K_a with the multiplier 83 to obtain neighboured correction data E_b (=$K_a . times . E_{ca}$). Step 5, 6 and 7 are same as those of FIG. 3. In STEP 8, the multiplier 84 calculates the product of the coefficient K_b and the average E_{ca} obtained in STEP 4 and adds the product to the difference between image signal level of the picture element O_{00} in the scanning window W_o and the binary image signal level from the comparator 7, which is calculated by the subtracter 81, in the adder 85 to produce renewed upper bit preference correction data E_{cu} and lower bit preference correction data E_{CL}. The renewed upper bit preference correction data E_{CU} is stored into address corresponding to the picture element E_{c5} in the scanning window W_e through the gate 87. STEP 9, 10 and 11 are same as those of FIG. 3. In this case, the error correction data E_a, the preference correction data E_{ca}, the upper bit preference correction data E_{CU} and lower bit preference correction data E_{CL} are cleared in every end of main scans in 11.

In this embodiment, the preference correction data E_{ca} may be replaced with average of the upper bit preference correction data E_{CU} as upper bits and average of the lower bit preference correction data E_{CL} as lower bits. The embodiment has advantages of saving the amount of buffer memory used as the correction data memory 29 from U+L bits to U bits.

FIG. 12 illustrates a sixth embodiment of the present invention. The embodiment is that combined with the embodiments of FIG. 8 and FIG. 10, and each of the components is same as that of FIG. 8 or FIG. 10 with same reference numeral. The operation is performed as illustrated in FIG. 13, which is the combination of FIG. 9 and FIG. 11. Therefore explanation is not repeated.

FIG. 14 illustrates a seventh embodiment of the present invention. An error data memory 31 and an error matrix 32 are same as the correction data memory 29 and the scanning window W_e of FIG. 10. Numeral 33 denotes memory location in which an error E_{xy} at co-ordinates xy of the original image is stored. An original image data I_{xy} from the co-ordinates xy of the original image is supplied to input terminal 35. An adder 36 calculates a sum $I'xy$ of the original image data Ixy and a mean error E_a. A comparator 39 compares the signal $I'xy$ with a predetermined value R/2 from a terminal 38 to obtain binary data Pxy=R when $I'xy > R/2$, and Pxy=0 when $I'xy . ltoreq . R/2$. The output Pxy from the comparator 39 is supplied to an output terminal 37. A subtracter 40 calculates the error Exy by subtracting the binary data Pxy from the signal $I'xy$. A weighted mean calculating means 41 calculates a weighted mean of error data stored in the error matrix 32 of the error data memory 31. Numeral 42 denotes a delay circuit.

The error data memory 31, the error matrix 32 and the weighted mean calculating means 41 correspond to the correction data memory 2P, the scanning window W_e and the average operator 82 of FIG. 10 respectively.

The weighted mean calculating means 41 calculates a weighted mean E_w of the data within the error matrix 32 by the following equation: ##EQU1## where, i and j are co-ordinates in the error matrix 32, and A_{ij} is a matrix coefficient which gives weights of distances from the co-ordinates xy of the referred picture element to the error. For example, A_{ij} is represented by: ##EQU2## where * is a location of the refered picture element. The mean error E_a consists of upper bits formed with the weighted mean E_w and lower bits formed with a lower L bits data $E_{x-1, y}$ (L) of the error $E_{x-1,y}$ which is obtained by delaying the error Exy from the subtractor 40 in the delay circuit 42. The adder 36 adds the mean error Ea and the original image data Ixy to obtain output $I'xy$ (=Ixy+Ea). The comparator 39 compares the output $I'xy$ of the adder 36 and the predetermined value R/2, and supplies the binary signal Pxy to the output terminal 37. The subtracter 40 calculates difference Exy of the output $I'xy$ of the adder 36 and the binary signal Pxy, and the upper U bit Exy(U) of the difference Exy is supplied to the error data memory 31 as a renewed error for the coordinate xy of the original image. The renewed error data Exy(U) is stored in the memory location 33 of the error data memory 31. On the other hand, the lower L bit Exy(L) of the difference Exy is supplied to the delay circuit 42. The delay circuit 42 replaces the data $E_{x-1,y}$ (L) before one picture element with the data Exy(L) and holds the same.

In calculating the mean error Ea, it is possible to add the output of the delay circuit 42 to a weighted mean which is obtained by calculating the same using the data consisted of upper U bit error data in the error matrix 32 and 0 added to lower L bits thereof. The method improves precision of calculating the weighted mean. Furthermore, the delay circuit 42

can be omitted by adjusting the subtractor 40 in holding previously subtracted results until the adder 36 receives the mean error Ea.

In experimental results, no deterioration of the reproduced image is observed by deleting lower 5 bit data from 8 bit data of the output Exy of the subtractor 40. On the contrally, a texture of a stripe pattern which is inherent to conventional mean error minimizing method is removed by delating the lower bit data. According to the embodiment of FIG. 14, the memory capacitance of the error data memory 31 can be reduced L bit per one picture element without deteriorating halftone reproducing characteristics.

【クレーム】

What is claimed is:

1. An apparatus for processing image signal comprising;
first and second image signal memory means for storing image signal levels of picture elements which are obtained by scanning an original image in a divided manner;
means for calculating a sum S of error correction data $E.sub.a$ and a sum $S.sub.m$ of the image signal levels of all picture elements within a first scanning window which has a size corresponding to M picture elements and which scans said first image signal memory means, and obtaining N and A from equation
$S=C.times.N+A$
where C is a predetermined image signal level, N is an integer falling in a range $O=N.ltoreq.M$, and A is an image signal level falling in a range $O.ltoreq.A<C$;
preference circuit means for numbering all picture elements to one of which neighboured correction data $E.sub.b$ is added, within a second scanning window which has a size corresponding to M picture elements so as to scan said second image signal memory means, in accordance with one of ascending and descending orders of the image signal levels;
rearrangement circuit means for assigning C as an image signal level to N picture elements of M picture elements in said first image signal memory means ordered by said preference circuit, A as an image signal level to a next picture element, and O as an image signal level to remaining picture elements,
means for comparing an image signal level of rearranged picture element with a predetermined quantizing level V for $O.ltoreq.V<C$, and for assigning C to the image signal level when the image signal level is greater than the quantizing level V as a binary image signal and assigning O to the image signal level when the image signal level is smaller than the quantizing level V as another binary image signal, and oprating the error correction data $E.sub.a$ from the difference of the image signal level and the assigned binary image signal,
third memory means for storing preference correction data,
a first calculating means for calculating the neiboured correction data $E.sub.b$ by the preference correction data neiboured to the refered picture element corresponding to that in said first or second scanning window and,
a second calculating means for calculating renewed preference correction data which are to be stored into add ress corresponding to the referred picture element with the preference correction data read out from said third memory, image signal level of the referred picture element in said second image signal memory and the binary image signal level.

2. An apparatus as claimed in claim 1, wherein said neighboured correction data $E.sub.b$ is calculated by multipying a coefficient $1/2.sup.n$ to a mean value of the preference correction data neighboured to the refered picture element, where n is an positive integer.

3. An apparatus as claimed in claim 1, wherein said renewed preference correction data is calculated by adding a product of a coefficient $11/2.sup.m$ and a mean value of the preference correction data neighboured to the refered picture element to a difference between said image signal level of the refered picture element in said second image signal memory and the binary image signal level, where m is an positive integer.

4. An apparatus as claimed in claim 1, further comprising an additive means for superposing to the image signal obtained by scanning the original image a signal having different signal level from said image signal.

5. An apparatus as claimed in claim 4, wherein said superposing signal is a periodical signal in synchronism with the picture element of said image signal.

6. An apparatus as claimed in claim 1, further comprising a selecting means for selecting output to be recorded and/or displayed, the selecting means comprises a comparator for comparing the image signal level of referred picture element with predetermined high and low reference levels, and a selector for selecting out a binary signal level or an output from said comparing means in accordance with the result obtained by said comparator.

7. An apparatus as claimed in claim 1, whrein said preference correction data neighboured to the referred picture element consists of upper U bit preference correction data and lower L bit preference correction data, and said third memory means stores said upper U bit preference correction data.

8. An apparatus as claimed in claim 1, wherein means are provided for operating preference correction data, said means

calculates a mean value of data consisting of the upper U bit preference correction data and 0 inserted into lower L bit, and adds the lower L bit preference correction data thereto.

9. An apparatus as claimed in claim 1, wherein means are provided for operating preference correction data, said means calculates a mean value of the upper U bit preference correction data as upper bit and adds the lower L bit preference correction data thereto as lower bit.

10. An apparatus for processing image signal comprising:

first image signal memory means for storing upper U bits data fo U+L bits image signal levels of picture elements which are obtained by scanning an original image in a divided manner;

second image signal memory means for storing U+L bits image signal levels of picture elements which are obtained by scanning an original image in a divided manner;

means for calculating a sum S of error correction data $E.sub.a$, valve Su consisting of a sum of the upper U bits data of M-1 picture elements within a first scanning window which has a size corresponding to M picture elements and which scans said first image signal memory means and 0 added to lower L bits, a rearrangement correction data S1 and image signal level of the original image, and obtaining N and A from equation

$S = C.times.N + A$

where C is a predetermined image signal level, N is an integer falling in a range $0.ltoreq.N.ltoreq.M$, and A is an image signal level falling in a range $0.ltoreq.A < C$;

preference circuit means for numbering all picture elements to one of which neighboured correction data $E.sub.b$ is added, within a second scanning window which has a size corresponding to M picture elements so as to scan said second image signal memory means, in accordance with one of ascending and descending orders of the image signal levels;

rearrangement circuit means for dividing said C, A and 0 into upper U bits data and lower L bits data and assigning the upper U bits of C as an image signal level to N picture elements of M-1 picture elements except predetermined rearranged one in said first image signal memory means ordered by said preference circuit, the upper U bits of A as an image signal level to a next picture element, and the upper U bits of 0 as an image signal level to remaining picture elements, for calculating a sum S, of the lower L bits of the image signal levels corresponding to said M-1 picture elements as a renewed rearrangement correction data, and for assiging all bits data to said predeterminal rearranged picture element, means for comparing an image signal level of rearranged picture element with a predetermined quantizing level V for $0.ltoreq.V < C$, and for assigning C to the image signal level when the image signal level is greater than the quantizing level V as a binary image signal and assigning 0 to the image signal level when the image signal level is smaller than the quantizing level V as another binary image signal, and operating the error correction data $E.sub.a$ from the difference of the image signal level and the assigned binary image signal,

third memory means for storing preference correction data,

a first calculating means for calculating the neighboured correction data $E.sub.b$ by the preference correction data neiboured to the referred picture element corresponding to that in said first or second scanning window and,

a second calculating means for calculating renewed preference correction data which are to be stored into address corresponding to the referred picture element with the preference correction data read out from said third memory, image signal level of the referred picture element in said second image signal memory and the binary image signal level.

11. An apparatus as claimed in claim 10, wherein said neighboured correction data $E.sub.b$ is calculated by multipying a coefficient $1/2.sup.n$ to a mean value of the preference correction data neighboured to the referred picture element, where n is an positive integer.

12. An apparatus as claimed in claim 10 wherein said renewed preference correction data is calculated by adding a product of a coefficient $11/2.sup.m$ and a mean value of the preference correction data neighboured to the refered picture element to a difference between said image signal level of the refered picture element in said second image signal memory and the binary image signal level, where m is an positive integer.

13. An apparatus as claimed in claim 10, wherein said preference correction data neighboured to the referred picture element consists of upper U bit preference correction data and lower L bit preference correction data, and said third memory means stores said upper U bit preference correction data.

14. An apparatus as claimed in claim 10, wherein means are provided for operating preference correction data said means calculates a mean value of data consisting of the upper U bit preference correction data and 0 inserted into lower L bit, and adds the lower L bit preference correction data thereto.

15. An apparatus as claimed in claim 10, wherein means are provided for operating preference correction data, said means calculates a mean value of the upper U bit preference correction data as upper bit and adds the lower L bit preference correction data thereto as lower bit.

16. An apparatus for processing image signal comprising:

a memory means for storing error data neighboured to a referred picture element xy, first calculating means for calculating a weighted mean value E_w of said error data neighboured to the referred picture element xy, second calculating means for adding original image data I_{xy} and a mean error E_a which consists of said weighted mean value E_w as upper bits and lower bits data $E_{x-1,y}(L)$ of the error data of one picture element before as lower bits to obtain a value $I'xy(=Ea+I'xy)$,

a comparator for comparing said value $I'xy$ with a predetermined value to obtain binary signal Pxy,

third calculating means for calculating a difference between said value $I'xy$ and binary signal Pxy as the error data Exy,

means for supplying upper U bits data of said error data Exy to said memory means, and

means for holding lower L bits data of said error data Exy until next picture element processing.

17. An apparatus as claimed in claim 16, wherein said weighted mean value E_w is calculated with data consisting of said error data as upper bits data and L bits 0 data inserted as lower bits data, and said mean error Ea is obtained by adding the thus obtained weighted mean value Ew and said lower bits clata $E_{x-1,y}(L)$ of the error data of one picture element before.